

Techno College of Engineering Agartala

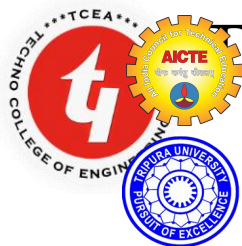
An Engineering College Approved by AICTE, MHRD, Govt. of India

Affiliated to Tripura University (A Central University),

Department of Electronics and Communication Engineering

List of Laboratory Experiments

| Digital Signal Processing Lab | | | | | | | |
|--|--|---|---|--|---------------|-----|---------|
| Course Code | Hours / Week | | | | Maximum Marks | | |
| PC EC 607 | L | T | P | C | CIA | SEE | Total |
| | 0 | 0 | 2 | 1 | 40 | 60 | 100 |
| Number of classes: 20-24 Hours | | | | Prerequisites: Engineering Mathematics | | | |
| Branch: ECE | | | | Semester: VI | | | |
| <p>Course overview:</p> <p>The Digital Signal Processing (DSP) Laboratory course provides practical exposure to fundamental and advanced concepts of DSP through hands-on experiments using MATLAB and DSP hardware platforms such as TMS320C50 or higher. The course emphasizes the implementation of signal generation, manipulation, and analysis techniques, along with filter design and real-time signal processing on DSP processors. Students will develop proficiency in applying theoretical DSP concepts to practical scenarios, including convolution, correlation, Z-transform, DFT/IDFT, circular convolution, and FIR/IIR filter design. The lab also introduces hardware-level programming and execution, fostering skills essential for digital communication, audio processing, and embedded DSP applications.</p> | | | | | | | |
| <p>Course objectives:</p> <ol style="list-style-type: none"> To develop competency in generating and manipulating discrete-time signals through programming and simulation using MATLAB or equivalent software. To impart practical knowledge of key DSP operations such as convolution, correlation, Z-transform, and frequency domain analysis using DFT and FFT algorithms. To provide hands-on experience in designing and implementing FIR and IIR filters, utilizing both software tools and DSP hardware platforms for real-time processing. To familiarize students with DSP hardware architecture and real-time execution, bridging the gap between theoretical concepts and practical embedded applications. | | | | | | | |
| <p>Course Outcomes:</p> | | | | | | | |
| CO Number | CO Description | | | | | | K-level |
| CO-1 | Make use of software to demonstrate generation of test signal and various signal operations. | | | | | | K-3 |
| CO-2 | Make use of software to demonstrate the convolution, correlation operations. | | | | | | K-3 |
| CO-3 | Analyse LTI system using software. | | | | | | K-4 |
| CO-4 | Develop program to compute Z-transform, inverse Z-transform, DFT, IDFT and circular convolution. | | | | | | K-6 |



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| CO-5 | Determine FIR and IIR filter in software. | K-5 |
| CO-6 | Develop FIR/IIR Filter design on digital signal processors. | K-3 |
| Perform at least 6 experiments (3 using Software simulation and 3 using DSP kit) | | |
| Perform the following exercises using suitable (Prefer MATLAB) software: | | |
| Sl. No. | EXPERIMENT NAME | CO |
| 1. | To develop elementary signal function modules for unit sample, unit step, unit ramp and exponential sequences. | CO-1 |
| 2. | To develop program modules based on operation on sequences like signal shifting, signal folding, signal addition and signal multiplication. | CO-1 |
| 3. | To develop program for discrete convolution and correlation. | CO-2 |
| 4. | To develop program for finding response of the LTI system described by the difference equation. | CO-3 |
| 5. | To develop program for computing Z transform and inverse Z-transform. | CO-4 |
| 6. | To develop program for computing DFT and IDFT. | CO-4 |
| 7. | To develop program for computing circular convolution. | CO-2 |
| 8. | To develop program for cascade realisation of IIR and FIR filters. | CO-5 |
| 9. | To develop program for designing FIR/IIR filter. | CO-5 |
| Perform the following exercises using TMS320C50 or Higher Board: | | |
| 1 | To study the architecture of DSP chips – TMS320C50 or higher. | |
| 2 | To verify linear convolution. | CO-2 |
| 3 | To verify the circular convolution. | CO-2 |
| 4 | To design FIR filter (LP/HP) using windowing technique a. Using rectangular window b. Using triangular window c. Using Kaiser window | CO-6 |
| 5 | To Implement IIR filter (LP/HP) on DSP Processors, N-point FFT algorithm. | CO-6 |