Techno College of Engineering Agartala

An Engineering College Approved by AICTE, MHRD, Govt. of India
Affiliated to Tripura University (A Central University),
Department of Electronics and Communication Engineering

List of Laboratory Experiments

VLSI Lab							
Course Code	**Hours / Week**				**Maximum Marks**		
PC EC-606	L	T	P	C	**CIA**	**SEE**	**Total**
	0	0	2	1	40	60	100
Number of classes: 24 Hours			**Prerequisites: Electronic Devices**				
Branch: ECE			**Semester: VI**				

Course overview:

This course provides practical experience in Very Large Scale Integration using CAD tools. Students will learn to analyze and simulate CMOS inverters and buffers at both circuit and layout levels, understanding their DC characteristics, delay, and power consumption. The lab also focuses on interpreting and implementing various combinational and sequential VLSI circuits. A significant component involves applying analytical and engineering skills to design and simulate a complete VLSI project, enhancing their practical understanding of modern VLSI design methodologies.

Course objectives:

i. To enable students to analyze and simulate CMOS inverter and buffer characteristics at the circuit level using CAD tools.
ii. To develop practical skills in analyzing CMOS inverter and buffer behavior at the layout level, understanding electrical aspects.
iii. To provide hands-on experience in interpreting and simulating various combinational and sequential VLSI circuits using CAD tools.
iv. To facilitate the application of analytical and engineering skills in a small VLSI project.

Course outcomes:

CO Number	CO Description	K-level
CO-1	Analyze a simulated CMOS inverter and Buffer at circuit level using CAD tool and be familiar with its various dc characteristics.	K-4
CO-2	Analyze a simulated CMOS inverter and Buffer at layout level using CAD tool and be familiar with its various electrical aspects and behavior.	K-4
CO-3	Interpret various combinational and sequential VLSI circuits using CAD tool.	K-2
CO-4	Build a small project where they can apply whole of their analytical and engineering skill that they learn throughout the course.	K-3

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Sl. No.	EXPERIMENT NAME	CO
1.	Simulation of logic gates using schematic & layout diagram by CAD tool.	CO-1
2.	Draw a schematic structure of CMOS inverter and buffer to evaluate its various characteristics like delay, power consumption, V-I characteristics, etc, by CAD tool.	CO-2
3.	Simulate a CMOS inverter and buffer using its layout diagram by CAD tool.	CO-2
4.	Simulation of combinational circuits using CAD tools.	CO-3
5.	Simulation of sequential circuits using CAD tools.	CO-3
6.	Simulation of counter using CAD tool.	CO-3
7.	Simulation of state machines using CAD tool.	CO-3
8.	Project (Simulation/ Implementation of VLSI circuit at schematic and layout level) using CAD tool.	CO-4