# Techno College of Engineering Agartala

An Engineering College Approved by AICTE, MHRD, Govt. of India
Affiliated to Tripura University (A Central University),
Department of Civil Engineering

## List of Laboratory Experiments

| Digital System Design Lab | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Course Code** | **Hours / Week** | | | | **Maximum Marks** | | |
| PC EC 507 | L | T | P | C | **CIA** | **SEE** | **Total** |
| | 0 | 0 | 2 | 1 | 40 | 60 | 100 |
| **Number of classes: 24 Hours** | | | **Prerequisites: Digital Electronics** | | | | |
| **Branch: ECE** | | | **Semester: V** | | | | |

**Course overview:**

The Digital System Design Lab is intended to provide hands-on experience in designing, simulating, and implementing digital logic circuits using both hardware (e.g., breadboards, ICs, FPGA boards) and software tools (e.g., Verilog, VHDL, simulation tools like ModelSim, Xilinx Vivado). Students will Understand the fundamentals of digital logic Design and test, combinational and sequential circuits.Write and simulate HDL code.Implement designs on FPGAs or CPLDs.

**Course objectives:**

1. **To develop a strong foundation in digital logic design:** Understand and analyze the behavior of basic logic gates, combinational and sequential circuits.

2. **To introduce Hardware Description Languages (HDL):** Learn to model digital systems using Verilog or VHDL at gate-level, dataflow, and behavioral abstraction levels.

3. **To provide hands-on experience with digital circuit implementation**Design and test digital circuits using simulation tools and implement them on hardware platforms like FPGAs or breadboards.

4. **To enable design of real-time digital systems:** Apply design methodologies to build systems such as counters, registers, ALUs, finite state machines, and display drivers.

**Course outcomes:**

| CO Number | CO Description | K-level |
|---|---|---|
| CO-1 | Demonstrate the Verilog HDL design flow to implement Logic Gates and Boolean function | K-2 |
| CO-2 | Develop Verilog HDL model of combinational logic circuits and implement them CPLD/FPGA | K-3 |
| CO-3 | Develop Verilog HDL model of sequential logic circuits and implement on CPLD/FPGA | K-3 |
| CO-4 | Construct State machines in Verilog HDL and implement on CPLD/FPGA | K-3 |
| **Sl. No.** | **EXPERIMENT NAME** | **CO** |
| 1. | Prepare Verilog HDL model to design and implement of the following digital circuits/systems on CPLD/FPGA platform. Logic gates and Boolean function | CO-1 |

| | | |
|---|---|---|
| 2. | Decoder and Encoder | CO-2 |
| 3. | Multiplexer and De-multiplexer | CO-2 |
| 4. | Full adder and Full subtractor | CO-3 |
| 5. | 8-bit Arithmetic logic unit | CO-3 |
| 6. | Flip flops, Counters | CO-4 |
| 7. | Universal shift register,Sequence detector | CO-2 |
| 8. | Traffic light controller | CO-4 |